What is claimed is:

1. A method of producing a layout pattern of a semiconductor device, comprising the steps of:

arranging primitive cells having circuit patterns of constituent elements of said semiconductor device in an element formation area of said semiconductor device; and

arranging at least one fill cell with a diffusion layer and no wiring, in vacant area that is generated after said primitive cells associated with all constituent elements of said semiconductor device have been arranged.

2. A method according to claim 1, wherein said fill cells are arranged such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device.

3. A method according to claim 1, wherein said fill cells are arranged such that a distribution ratio falls within the range 30 - 55% in said element formation area, said distribution ratio being the proportion of said diffusion layers that are distributed in said element formation area of said semiconductor device.

4. A method according to claim 1, wherein a plurality of types of fill cells having different sizes that are each identified by an identifier having the same amount of information are prepared and are arranged in said vacant area in order of size starting from the largest fill cells that can be arranged in said vacant area.

5. A method according to claim 1, wherein said constituent

elements are grouped such that constituent elements having related operation are sorted into the same group; and said primitive cells associated with constituent elements that belong to the same group are arranged in proximity.

6. A method according to claim 1, further comprising a step of producing mask data for fabricating a reticle to be used in fabricating said semiconductor device, from a layout pattern in which said primitive cells and said fill cells are arranged.

7. A device of producing a layout pattern of a semiconductor device, comprising:

a netlist storage unit for storing a netlist composed of data indicating constituent elements of said semiconductor device and the connection relationship thereof;

a library storage unit for storing data of: primitive cells having the circuit patterns of said constituent elements, and fill cell with diffusion layers and no wiring that is arranged in vacant area generated after said primitive cells have been arranged; and

a processor for referring to said netlist storage unit and said library storage unit, arranging said primitive cells in the element formation area of said semiconductor device, and arranging at least one said fill cell in vacant area generated after said primitive cells associated with all constituent elements of said semiconductor device have been arranged.

8. A device according to claim 7, wherein said processor arranges said fill cells such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device.

9. A device according to claim 7, wherein said processor arranges said fill cell such that the distribution ratio falls within the range 30 - 55% in said element formation area, said distribution ratio being the proportion of said diffusion layers that are distributed in said element formation area of said semiconductor device.

10. A device according to claim 7, wherein:

said library storage unit stores a plurality of types of fill cells having different sizes and that are each identified by an identifier having the same amount of information; and

said processor refers to said library storage unit and arranges fill cell in said vacant area in order of size starting from the largest fill cells that can be arranged in said vacant area.

11. A device according to claim 7, wherein:

said netlist storage unit stores group information that indicate groups composed of constituent elements having related operations; and

said processor refers to said netlist storage unit and, based on said group information, arranges said primitive cells associated with constituent elements which belong to the same group in proximity.

12. A device according to claim 7, wherein said processor makes mask data for fabricating a reticle for fabricating said semiconductor device from a layout pattern in which said primitive cells and said fill cell are arranged.

13. A method of fabricating a semiconductor device in which

diffusion layers and trenches for isolating elements are formed on a wafer, following which an insulating film is formed over the entire surface of said wafer including the interior of said trenches, and said insulating film is ground to planarize the surface of said wafer; said method comprising the steps of:

forming primitive cells having circuit patterns of constituent elements of said semiconductor device in the element formation area of said semiconductor device; and

forming at least one fill cell with a diffusion layer and no wiring, in vacant area that is generated after forming said primitive cells associated with all constituent elements of said semiconductor device.

14. A method according to claim 13, wherein said fill cell is formed such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device.

15. A method according to claim 13, wherein said fill cell is formed such that the distribution ratio falls within the range 30 - 55% in said element formation area, said distribution ratio being the proportion of said diffusion layers that are distributed in said element formation area of said semiconductor device.

16. A method according to claim 13, wherein:

said constituent elements are grouped such that constituent elements having related operations are sorted into the same group; and

said primitive cells associated with constituent elements that belong to the same group are formed in proximity.